

IN THE CLAIMS:

Please note that all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity. No amendments have been made herein.

1. (Previously Amended) A semiconductor device comprising:

at least one layer of boro-phospho silicate glass; and

at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of said at least one layer of boro-phospho silicate glass.

2. A semiconductor device comprising:

a plurality of layers of boro-phospho silicate glass; and

a plurality of layers of germanium boro-phospho silicate glass, at least a portion of at least one layer of said plurality of layers of germanium boro-phospho silicate glass contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

3. (Previously Amended) A semiconductor device comprising:

a plurality of layers of boro-phospho silicate glass; and

a plurality of layers of germanium boro-phospho silicate glass, each layer of said plurality of layers of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

4. (Previously Amended) A semiconductor memory device comprising:

at least one layer of boro-phospho silicate glass; and

at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of said at least one layer of boro-phospho silicate glass.

5. A semiconductor memory device comprising:  
a plurality of layers of boro-phospho silicate glass; and  
a plurality of layers of germanium boro-phospho silicate glass, at least a portion of at least one layer of said plurality of layers of germanium boro-phospho silicate glass contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

6. (Previously Amended) A semiconductor memory device comprising:  
a plurality of layers of boro-phospho silicate glass; and  
a plurality of layers of germanium boro-phospho silicate glass, each layer of said plurality of layers of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

7. (Previously Amended) A semiconductor memory device comprising:  
at least one capacitor cell having a portion thereof formed by at least one layer of boro-phospho silicate glass and at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of said at least one layer of boro-phospho silicate glass.

8. A semiconductor memory device comprising:  
at least one capacitor cell having a portion thereof formed by a plurality of layers of boro-phospho silicate glass and a plurality of layers of germanium boro-phospho silicate glass, at least a portion of at least one layer of said plurality of layers of germanium boro-phospho silicate glass contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

9. A semiconductor memory device comprising:

at least one capacitor cell having a portion thereof formed by a plurality of layers of boro-phospho silicate glass and a plurality of layers of germanium boro-phospho silicate glass, each layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

10. (Previously Amended) The memory device of claim 9, further comprising:

at least one dielectric layer; and  
a conductive layer over said at least one dielectric layer.

11. (Previously Amended) The memory device of claim 10, wherein said at least one dielectric layer comprises one of  $\text{Si}_3\text{N}_4$ ,  $\text{Ta}_2\text{O}_5$ , or BST.

12. (Previously Amended) The memory device of claim 10, wherein said conductive layer comprises Si-Ge.

13. (Previously Amended) The memory device of claim 9, further comprising:

at least one dielectric layer covering at least portions of said plurality of layers of boro-phospho silicate glass and said plurality of layers of germanium boro-phospho silicate glass; and  
a conductive layer covering at least a portion of said at least one dielectric layer.